DESCRIPTION

The VP8075 series of devices are highly integrated Li-ion linear chargers and system power path management devices targeted at space-limited portable applications. The devices operate from either a USB port or AC adapter. The high input voltage range with input overvoltage protection supports low-cost unregulated adapters.

The VP8075 offer DC supply power-path management with autonomous power-source selection, power FETs and current sensors, high-accuracy current and voltage regulation, charge status, and charge termination, in a single monolithic device.

The VP8075 power the system while independently charging the battery. This feature reduces the charge and discharge cycles on the battery, allows for proper charge termination and allows the system to run with an absent or defective battery pack. This feature also allows for the system to instantaneously turn on from an external power source in the case of a deeply discharged battery pack. The IC design is focused on supplying continuous power to the system when available from the AC adapter or battery sources.

FEATURES

- Integrated Power-Path Management Feature Simultaneously and Independently Powers the System and Charges the Battery
- Integrated USB Charge Control with Selectable 100mA and 500mA Maximum Input Current Ensures Compliance to USB-IF Standard
- Supports Up to 1.4 Amps Charge Current
- 24V Input Rating
- Thermal Regulation for Charge Control
- Programmable Pre-Charge and Fast-Charge Safety Timers
- Reverse Current, Short-Circuit, and Thermal Protections
- Status Indicator-Charging, Done, Power Good
- 3mm×3mm TQFN-16 Package
- RoHS Compliant and 100% Lead (Pb)-Free Halogen-Free

APPLICATION

- Smart Phones and PDA
- MP3 Players
- Digital Cameras and Handheld Devices
- Internet Appliances

Typical Application Circuit

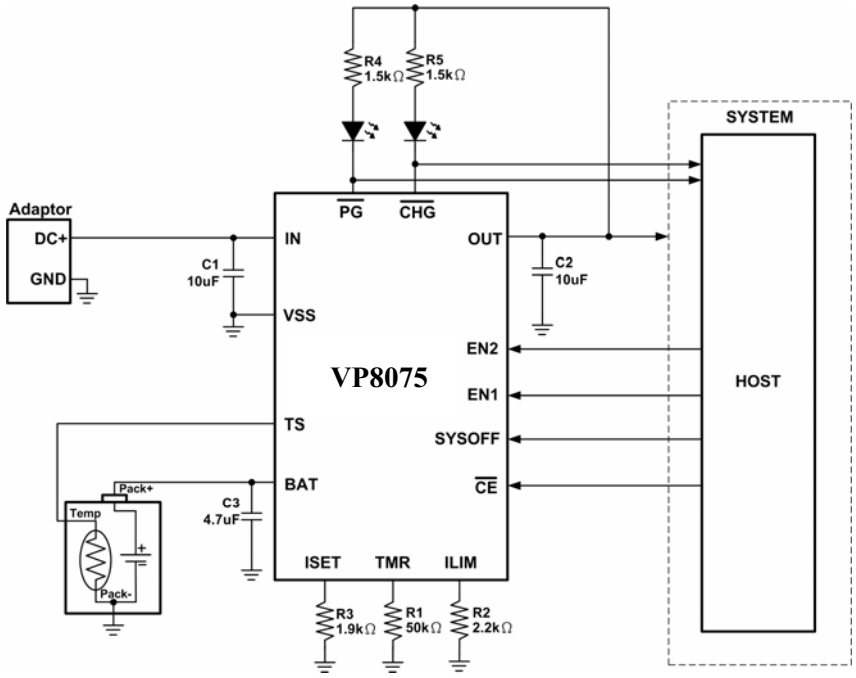


Figure 1.

Simplified Power Flow Diagram

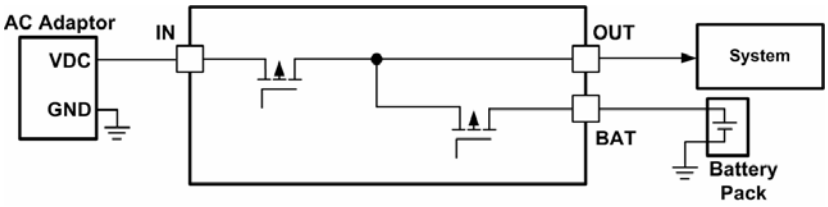


Figure 2.

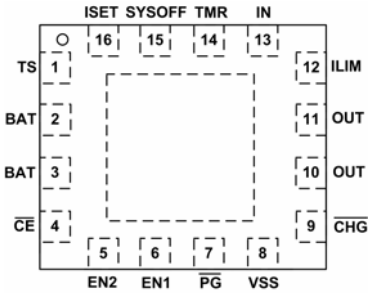
DESCRIPTION (continued)

The charger power stage and charge current sense functions are fully integrated. The charger function has high accuracy current and voltage regulation loops, charge status display, and charge termination. The input current limit and charge current are programmable using external resistors.

Table 1. EN1/EN2 Settings

EN2	EN1	Maximum Input current into IN pin
0	0	100mA. USB 100 mode
0	1	500mA. USB 500 mode
1	0	Set by an external resistor from ILIM to VSS
1	1	Standby (USB suspend mode)

Pin Configurations

Package Type	Pin Configurations
TQFN-16	

Pin Description

PIN	TQFN-16	I/O	DESCRIPTION
TS	1	I	Temperature sense input
BAT	2,3	I/O	Battery input and output
$\overline{CE}$	4	I	Charge Enable Active-Low Input. Connect CE to a high logic level to place the battery charger in standby mode. In standby mode, OUT is active. Connect CE to a low logic level to enable the battery charger.
EN2	5	I	Charge current set point for USB port. EN1 (High=500mA, Low=100mA) Input Current Limit Configuration . Use EN1 and EN2 control the maximum input current and enable USB compliance. See Table 1 for the description of the operation states.
EN1	6	I	
$\overline{PG}$	7	O	Power-good status output (open-drain)
VSS	8	-	Ground input
$\overline{CHG}$	9	O	Charge status output (open-drain)
OUT	10,11	O	Output terminal to the system

Pin Description (continued)

PIN	TQFN-16	I/O	DESCRIPTION
ILIM	12	I	Adjustable Current Limit Programming Input. Connect a resistor from ILIM to VSS to program the maximum input current (EN2=1, EN1=0). The input current includes the system load and the battery charge current.
IN	13	I	Charge input voltage
TMR	14	I	Timer Programming Input. TMR controls the pre-charge and fast-charge safety timers. Connect TMR to VSS to disable all timers. Connect a resistor between TMR and VSS to program the timers a desired length. Leave TMR unconnected to set the timers to the default values.
ISET	16	I/O	Charge current set point and precharge and termination set point
SYSOFF	15	I	Connect SYSOFF high to disconnect OUT from BAT. Internally pulled up to VBAT through a large resistor.

Ordering Information

Order Number	Package Type	Marking	Operating Temperature Range	V_{OVP}	$V_{OUT(REG)}$	V_{DPM}	OPTIONAL FUNCTION
VP8075JIR1	TQFN-16	xxxxx P8075	-40°C to +85°C	6.6V	5.5V	4.3V	SYSOFF

VP8075 □ □ □ □

Lead Free Code
1: Lead Free, Halogen Free 0: Lead

Packing
R: Tape & Reel

Operating temperature range
I: Industry Standard

Package Type
J: TQFN

Block Diagram

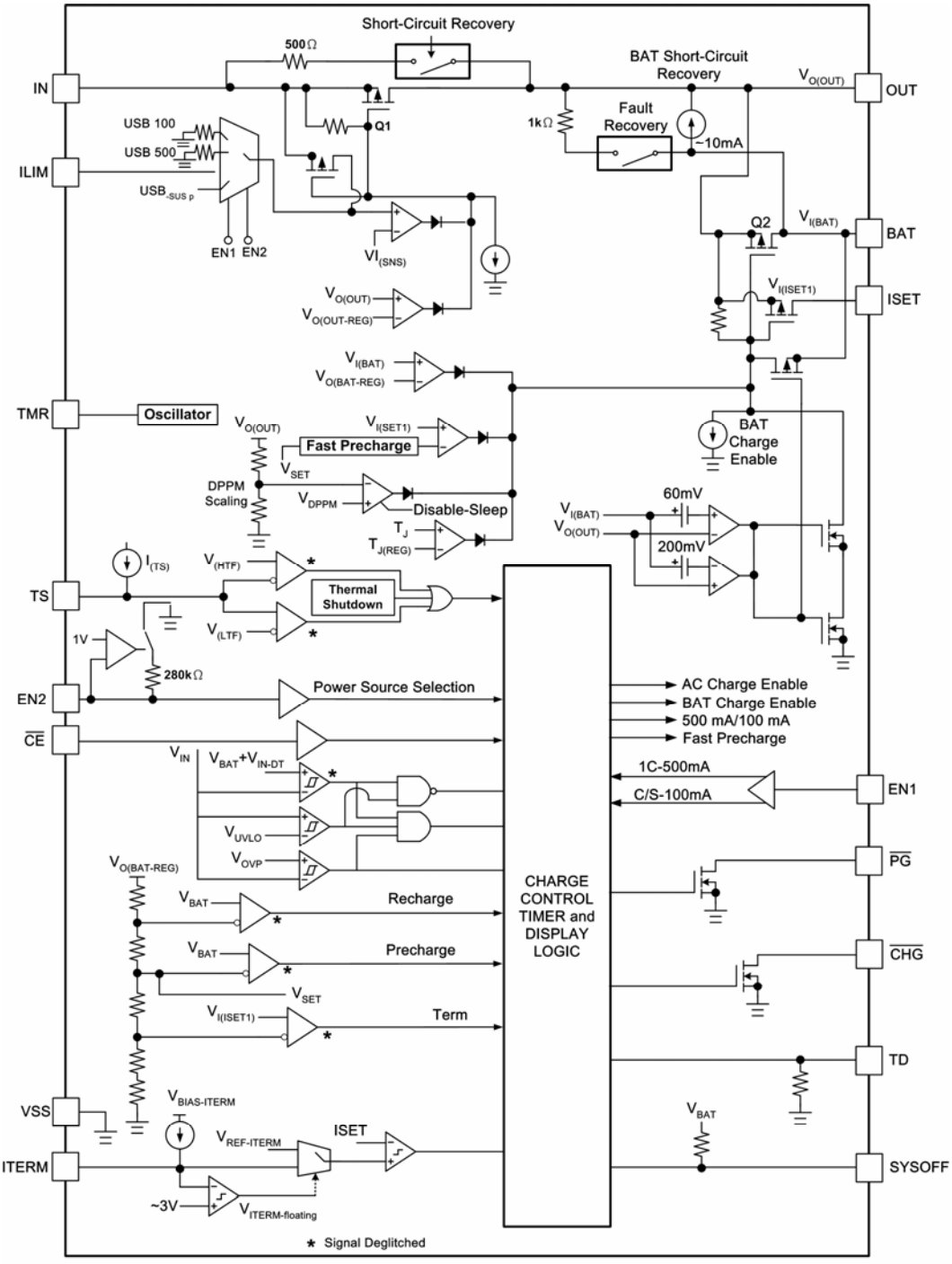


Figure 3. Block Diagram

Absolute Maximum Ratings

- Input voltage IN(DC voltage with respect to VSS)---------- -0.3V to 24V
- Input Voltage on BAT, $\overline{CE}$, $\overline{PG}$, EN2, OUT, ISET, EN1, $\overline{CHG}$, TS, ILIM, SYSOFF, TMR (all DC Voltages VSS) ---------- -0.3V to 7V
- Input Current ---------- 1.6A
- Output Current (OUT pin) ---------- 1.6A
- Output Current (BAT) ---------- 1.4A
- Output Sink Current ($\overline{PG}$, $\overline{CHG}$) ---------- 15mA
- Junction temperature range, T_J ---------- 150°C
- Storage temperature range, Tstg ---------- -65°C to 150°C
- Lead temperature (soldering, 10s) ---------- 260°C

Recommended Operating Conditions

	Min.	Max.	Unit
Supply voltage, V_{IN}	4.35	24	V
Operating junction temperature range, T_J	-40	125	°C

Electrical Characteristics

over junction temperature range (0°C ≤ T_A ≤85°C) and the recommended supply voltage range (unless otherwise noted).

SYMBOLE	PARAMETER	TEST CONDITIONS	VP8075			
			MIN	TYP	MAX	UNIT
INPUT BIAS CURRENTS						
$I_{CC(SPLY)}$	Active supply current, IN pin	$\overline{CE}$ =Low, V_{IN}=6V, No Load on OUT pin, V_{BAT}>$V_{O(BAT\_REG)}$ (EN1,EN2) ≠ (HI, HI)		1	1.5	mA
$V_{(SLPENT)}$	Sleep-mode entry threshold	V_{BAT}=4V, V_{IN}: 4.4V→ 3.9V		60		mV
$V_{(SLPEXIT)}$	Sleep-mode exit threshold	Input power detected V_{BAT}=4V, V_{IN}: 3.9V→ 4.4V		160		mV
I_{IN}	Standby current into IN pin	EN1=High, EN2=High, V_{IN}=6V			250	µA
V_{OVP}	Input overvoltage protection threshold	V_{IN}: 5V → 7V	6.4	6.6	6.9	V
$I_{BAT(PDWN)}$	Sleep current into BAT pin	$\overline{CE}$ =Low or HI, input power not detected, No load on OUT pin			7	µA
$V_{IN(DPM)}$		EN2=0, EN1=X	4.55	4.65	4.8	V
OUT PIN-VOLTAGE REGULATION						
$V_{O(REG)}$	Output pin voltage regulation	V_{IN}>V_{OUT}+V_{DO}	5.3	5.5	5.6	V
OUT PIN- DPPM REGULATION						
V_{DPPM}			4.2	4.3	4.4	V
BAT PIN CHARGING-PRECHARGE						
$V_{(LOWV)}$	Precharge to fast-charge transition		2.9	3	3.1	V
$K_{(PRECHG)}$	Precharge current factor		70	96	116	AΩ
BAT PIN CHARGING-CURRENT REGULATION						
$I_{O(BAT)}$	AC battery charge current range (1)	$V_{I(BAT)}$ > $V_{(LOWV)}$, EN2=High, EN1=Low $I_{O(BAT)}$ = ($K_{(SET)}$ / R_{SET}),	400	1000	1400	mA
$K_{(SET)}$	Charge current factor		840	962	1070	AΩ
USB MODE INPUT CURRENT LIMIT						
I_{IN}max	Maximum input current	EN1=Low, EN2=Low	70	90	100	mA
		EN1=High, EN2=Low	390	440	500	
		EN2=High, EN1=Low		K_{ILIM} /R_{ILIM}		A
K_{ILIM}	Maximum input current factor			1650		AΩ
I_{IN}max	Programmable input current limit range	EN2=High, EN1=Low	200		1500	mA

Electrical Characteristics (continued)

over junction temperature range (0°C ≤ T_A ≤85°C) and the recommended supply voltage range (unless otherwise noted).

SYMBOLE	PARAMETER	TEST CONDITIONS	VP8075			
			MIN	TYP	MAX	UNIT
OUT PIN-SHORT CIRCUIT						
I_{OSHI}	BAT to OUT short-circuit recovery	Current source between BAT to OUT for short-circuit recovery to $V_{I(OUT)} \leqq V_{I(BAT)}$-200mV		10		mA
BAT PIN CHARGING VOLTAGE REGULATION						
$V_{O(BAT-REG)}$	Battery charge voltage			4.2		V
	Battery charge voltage regulation accuracy	T_J = 25°C	–0.5%		0.5%	
		T_J = 0°C ~85°C	–1%		1%	
CHARGE TERMINATION DETECTION						
$V_{(TERM)}$	Charge termination set voltage , measured on ISET	$V_{I(BAT)}$>$V_{(RCH)}$,EN2=High	230	250	270	mV
		$V_{I(BAT)}$>$V_{(RCH)}$,EN1=High	60	80	100	
TEMPERATURE SENSE COMPARATORS						
V_{LTF}	High voltage threshold	Temp fault at V(TS)> V_{LTF}	2	2.1	2.2	V
V_{HTF}	Low voltage threshold	Temp fault at V(TS)< V_{HTF}	0.27	0.30	0.33	V
I_{TS}	Temperature sense current source		70	80	90	μA
BATTERY RECHARGE THRESHOLD						
V_{RCH}	Recharge threshold voltage		$V_{O(BAT-REG)}$ -0.05	$V_{O(BAT-REG)}$ -0.100	$V_{O(BAT-REG)}$ -0.150	V
$\overline{CHG}$, AND $\overline{PG}$, OPEN DRAIN (OD) OUTPUTS (2)						
V_{OL}	Low-level output saturation voltage	I_{OL} = 5 mA , An external pullup resistor ≥1K required.			0.4	V
EN1,EN2, $\overline{CE}$,SYSOFF INPUTS						
V_{IL}	Low-level input voltage		0		0.4	V
V_{IH}	High-level input voltage		1.4		5	
TIMERS						
$K_{(TMR)}$	Timer set factor	$t_{(CHG)}$=$K_{(TMR)}$ × $R_{(TMR)}$	0.313	0.360	0.414	s/Ω
$R_{(TMR)}$	External resistor limits		30		100	kΩ
$t_{(PRECHG)}$	Precharge timer			0.10×$t_{(CHG)}$		s
THERMAL SHUTDOWN REGULATION (3)						
$T_{(SHTDWN)}$	Temperature trip	T_J (Q1 and Q3 only)		155		°C
	Thermal hysteresis	T_J (Q1 and Q3 only)		10		
$T_{J(REG)}$	Temperature regulation limit	T_J (Q2)		130		
UVLO						
$V_{(UVLO)}$	Undervoltage lockout	Decreasing V_{IN}	2	2.2	2.6	V

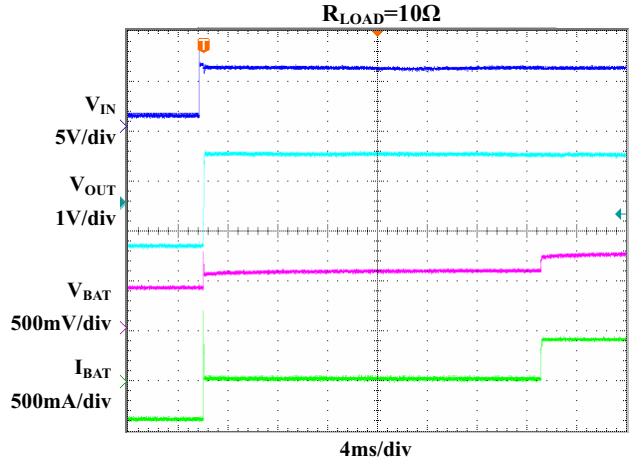
(1) When input current remains below 1.4A, the battery charging current may be raised until the thermal regulation limits the charge current.

(2) See Charger Sleep mode for $\overline{PG}$ specifications.

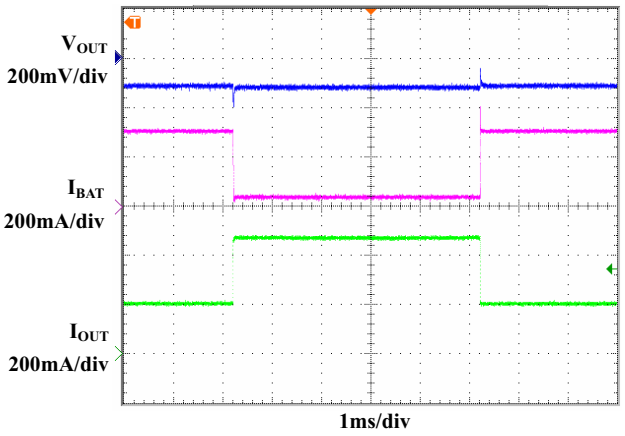
(3) Reaching thermal regulation reduces the charging current. Battery supplement current is not restricted by either thermal regulation or shutdown. Input power FETs turn off during thermal shutdown. The battery FET is only protected by a short-circuit limit which typically does not cause a thermal shutdown (input FETs turning off) by itself.

Typical Operating Characteristics

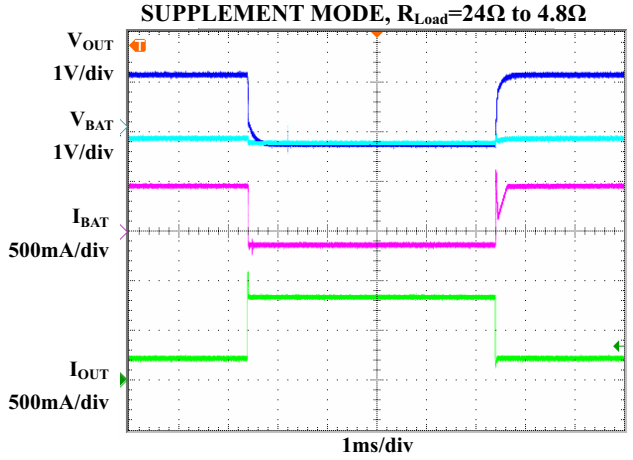
ADAPTER PLUG-IN BATTERY CONNECTED
R_{LOAD}=10Ω



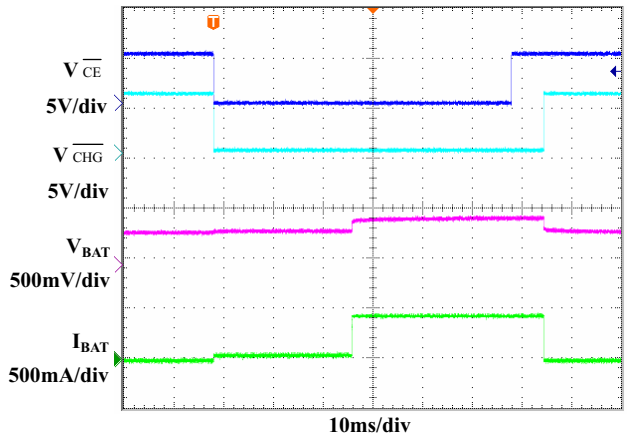
DPPM MODE, R_{Load}=20Ω to 9Ω



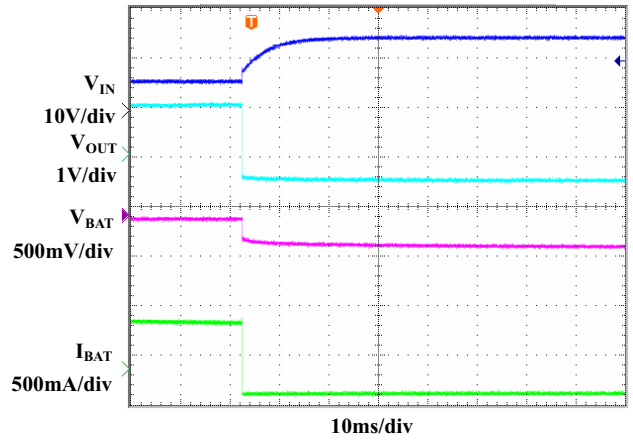
ENTERING AND EXITING BATTERY SUPPLEMENT MODE, R_{Load}=24Ω to 4.8Ω



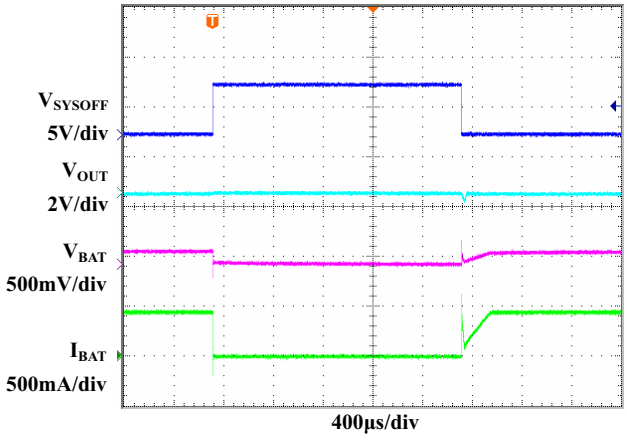
CHARGER ON/OFF USING $\overline{CE}$



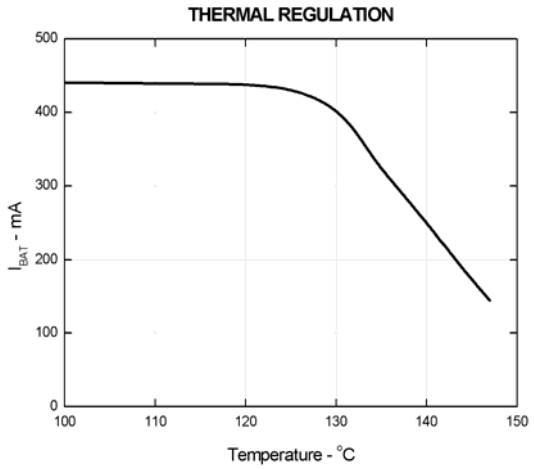
OVP FAULT, VIN=6V to15V, R_{Load}=10Ω

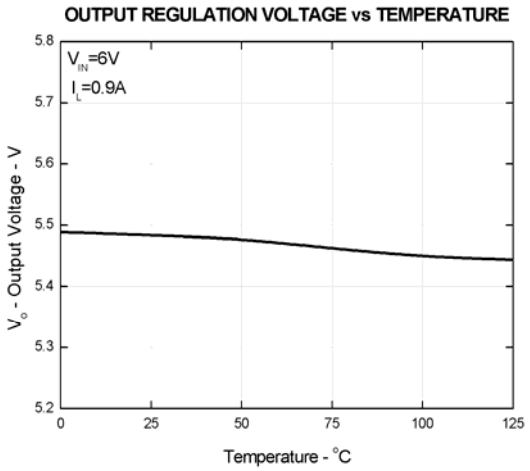


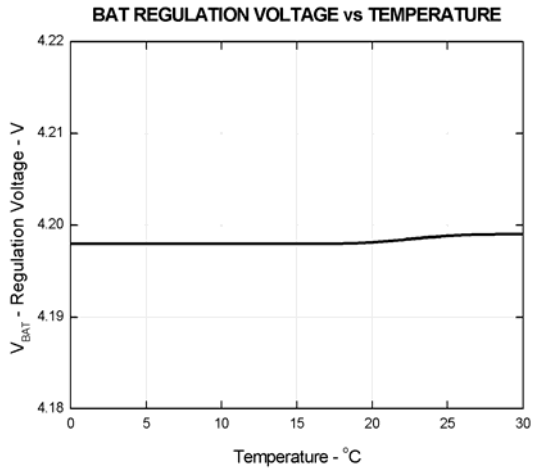
SYSTEM ON/OFF with INPUT CONNECTED

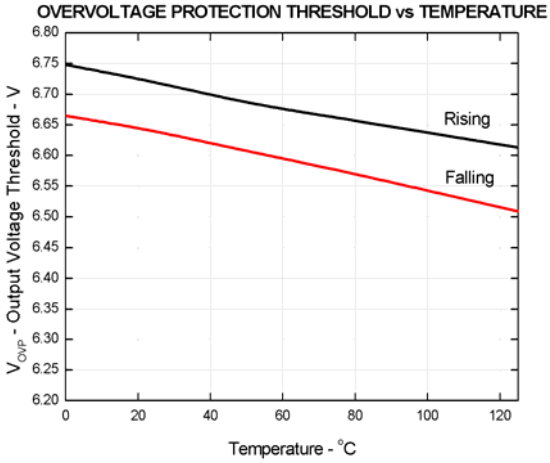


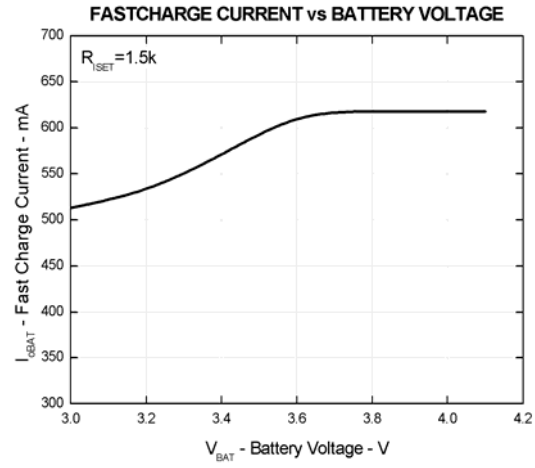
Typical Operating Characteristics (continued)

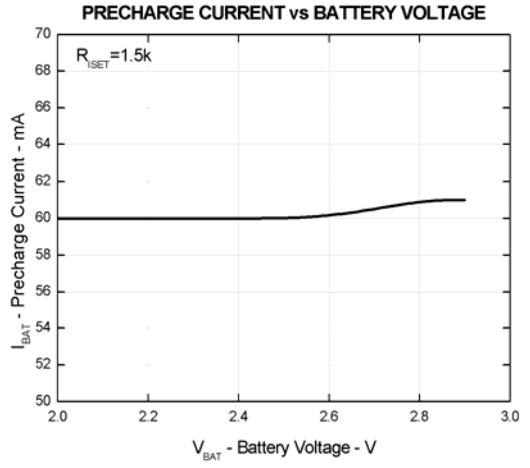












Flow Chart

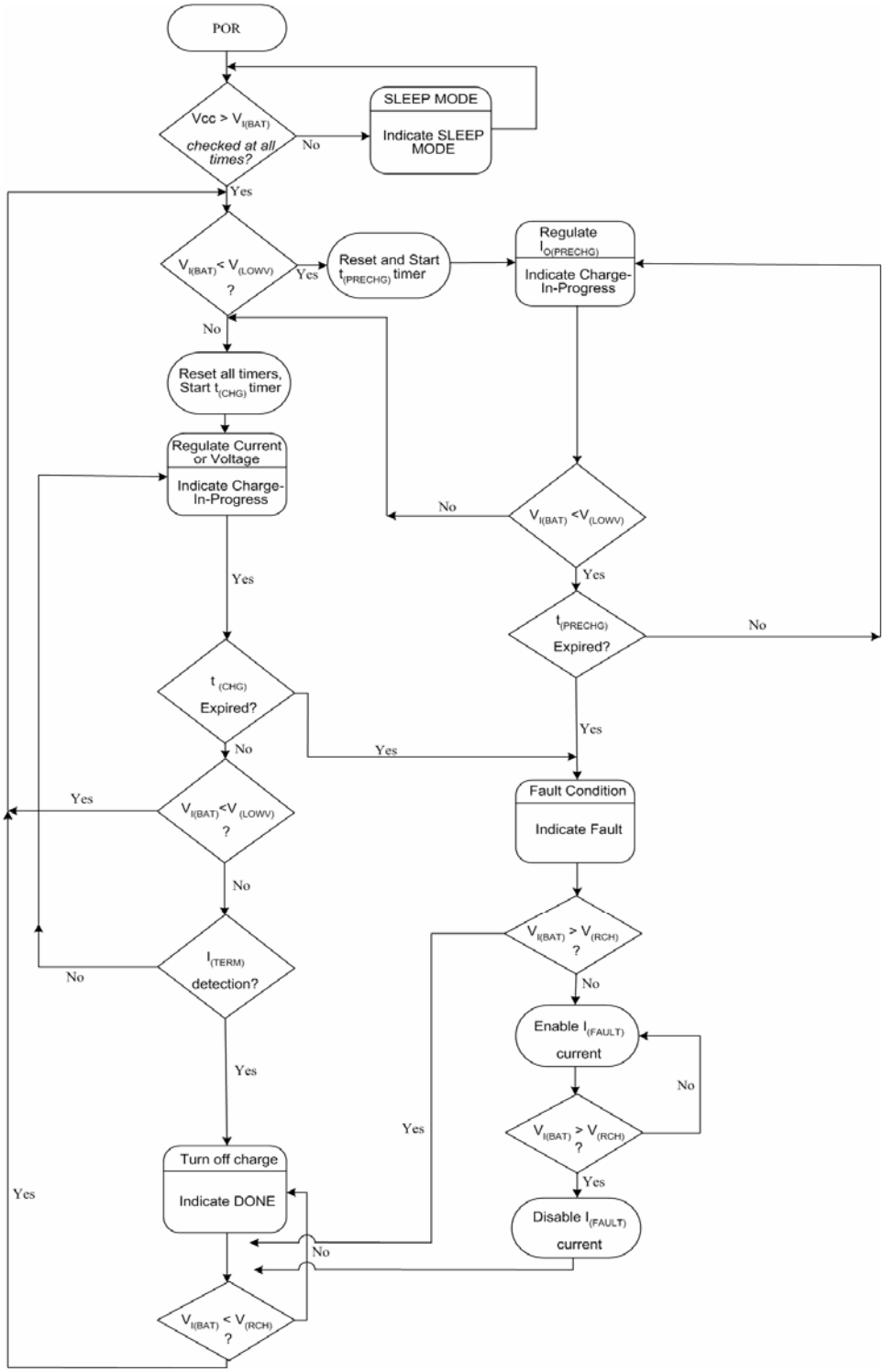


Figure 4. Operational Flow Chart

FUNCTIONAL DESCRIPTION

Autonomous Power Source Selection, Mode Control Pin

With the EN2 input low, the VP8075 defaults to USB-mode charging, and the supply current is limited by the EN1 pin (100 mA for EN1 = Low, 500 mA for EN1= High). If an input source is not available, then the battery is selected as the source.

Power-Path Management

The VP8075 powers the system while independently charging the battery. This feature reduces the charge and discharge cycles on the battery, allows for proper charge termination, and allows the system to run with an absent or defective battery pack. This feature gives the system priority on input power, allowing the system to power up with a deeply discharged battery pack. This feature works as follows:

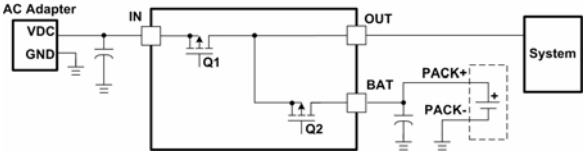


Figure 5. Power-Path Management

Case 1: AC Mode (EN2= High)

System Power

In this case, the system load is powered directly from the AC adapter through the internal transistor Q1. The output is regulated at 5.5V. If the system load exceeds the capacity of the supply, the output voltage drops down to the battery's voltage.

Charge Control

When in AC mode the battery is charged through switch Q2 based on the charge rate set on the ISET input.

Dynamic Power-Path Management (DPPM)

This feature monitors the output voltage (system voltage) for input power loss due to brown outs, current limiting, or removal of the input supply. If the voltage on the OUT pin drops to a preset value, due to a limited amount of input current, then the battery charging current is reduced until the output voltage stops dropping. The DPPM control tries to reach a steady-state condition where the system gets its needed current and the battery is charged with the remaining current. Therefore, if the system demands more current than the input can provide, the output voltage drops just below the battery voltage and Q2 turns on which supplements the input current to the system. DPPM has three main advantages.

1. This feature allows the designer to select a lower power wall adapter. The smaller adaptor's voltage drops until the output voltage reaches the DPPM regulation voltage threshold. The charge current is reduced until there is no further drop on the output voltage.
2. Using DPPM provides a power savings compared to configurations without DPPM. Without DPPM, if the system current plus charge current exceed the supply's current limit, then the output is pulled down to the battery. Linear chargers dissipate the unused power $(V_{IN}-V_{OUT}) \times I_{LOAD}$. The current remains high (at current limit) and the voltage drop is large for maximum power dissipation. With DPPM, the voltage drop is less $(V_{IN}-V_{(DPPM-REG)})$ to the system which means better efficiency. The efficiency for charging the battery is the same for both cases. The advantages include less power dissipation, lower system temperature, and better overall efficiency.
3. The DPPM sustains the system voltage no matter what causes it to drop, if at all possible. It does this by reducing the noncritical charging load while maintaining the maximum power output of the adaptor.

The safety timer is dynamically adjusted while in DPPM mode. The voltage on the ISET pin is directly proportional to the programmed charging current. When the programmed charging current is reduced, due to DPPM, the ISET and TMR voltages are reduced and the timer's clock is proportionally slowed, extending the safety time. In normal operation V(TMR) = 2.5V; and, when the clock is slowed, V(TMR) is reduced. When V(TMR) = 1.25V, the safety timer has a value close to 2 times the normal operation timer value.

Case 2: USB Mode (EN2 = Low)

System Power

In this case, the system load is powered from a USB port through the internal switch Q1. Note that in this case, Q1 regulates the total current to the 100-mA or 500-mA level, as selected on the EN1 input. The system's power management is responsible for keeping its system load below the USB current level selected (if the battery is critically low or missing). Otherwise, the output drops to the battery voltage; therefore, the system should have a low-power mode for USB power application.

The DPPM feature keeps the output from dropping below its programmed threshold, due to the battery charging current, by reducing the charging current.

Charge Control

When in USB mode, Q1 regulates the input current to the value selected by the EN1 pin (0.1/0.5A). The charge current to the battery is set by the ISET resistor (typically > 0.5A). Because the charge current typically is programmed for more current than the USB current limit allows, the output voltage drops to the battery voltage or DPPM voltage, whichever is higher. If the DPPM threshold is reached first, the charge current is reduced until V_{OUT} stops dropping. If V_{OUT} drops to the battery voltage, the battery is able to supplement the input current to the system.

Dynamic Power-Path Management (DPPM)

The theory of operation is the same as described in CASE 1, except that Q1 is restricted to the USB current level selected by the EN1 pin.

With a source connected, the power-path management circuitry of the VP8075 monitors the input current continuously. The OUT output for the VP8075 is regulated to a fixed voltage ($V_{O(REG)}$). The current into IN is shared between charging the battery and powering the system load at OUT. The VP8075 has internal selectable current limits of 100mA (USB100) and 500mA (USB500) for charging from USB ports, as well as a resistor- programmable input current limit.

The input current limit selection is controlled by the state of the EN1 and EN2 pins as shown in Table 1. When using the resistor-programmable current limit, the input current limit is set by the value of the resistor connected from the ILIM pin to VSS, and is given by the equation:

$$I_{IN-MAX} = \frac{K_{ILIM}}{R_{ILIM}} \quad (1)$$

Battery Temperature Monitoring

The VP8075 continuously monitors battery temperature by measuring the voltage between the TS and VSS pins. An internal current source provides the bias for most-common 10kΩ negative-temperature coefficient thermistors (NTC) (see Figure 6). The device compares the voltage on the TS pin against the internal $V_{(LTF)}$ and $V_{(HTF)}$ thresholds to determine if charging is allowed. Once a temperature outside the $V_{(LTF)}$ and $V_{(HTF)}$ thresholds is detected, the device immediately suspends the charge. The device suspends charge by turning off the power FET and holding the timer value (i.e., timers are not reset). Charge is resumed when the temperature returns to the normal range. However, the user may increase the range by adding two external resistors. See Figure 7.

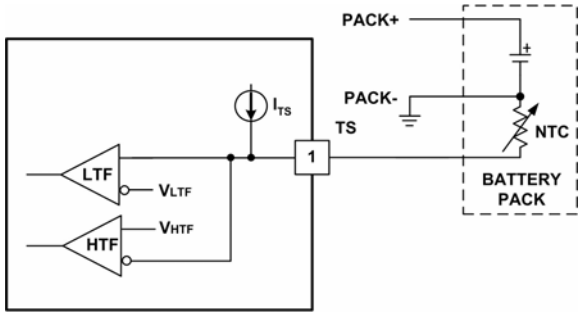


Figure 6. TS Pin Configuration

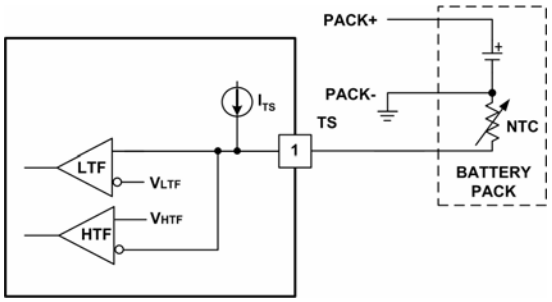


Figure 7. TS Pin Thresholds

Battery Pre-Conditioning

During a charge cycle, if the battery voltage is below the $V_{(LOWV)}$ threshold, the VP8075 applies a precharge current, $I_{O(PRECHG)}$, to the battery. This feature revives deeply discharged cells. The resistor connected between the ISET and VSS, R_{SET}, determines the precharge rate. The $K_{(SET)}$ parameters are specified in the specifications table. Note that this applies to both AC-mode and USB-mode charging.

$$I_{O(PRECHG)} = \frac{K_{(PRECHG)}}{R_{SET}} \quad (2)$$

The VP8075 activates a safety timer, $t_{(PRECHG)}$, during the conditioning phase. If $V_{(LOWV)}$ threshold is not reached within the timer period, the VP8075 turns off the charger and enunciates FAULT on the $\overline{CHG}$. The timeout is extended if the charge current is reduced by DPPM or thermal regulation.

Battery Charge Current

The VP8075 offers on-chip current regulation with programmable set point. The resistor connected between the ISET and VSS, RSET, determines the charge level. The charge level may be reduced to give the system priority on input current (see DPPM). The $K_{(SET)}$ parameters are specified in the specifications table.

$$I_{O(BAT)} = \frac{K_{(SET)}}{R_{SET}} \quad (3)$$

When powered from a USB port, the input current available (0.1A/0.5A) is typically less than the programmed (ISET) charging current, and therefore, the DPPM feature attempts to keep the output from being pulled down by reducing the charging current.

Battery Voltage Regulation

The voltage regulation feedback is through the BAT pin. This input is tied directly to the positive side of the battery pack. The VP8075 monitors the battery-pack voltage between the BAT and VSS pins. When the battery voltage rises to the $V_{O(BAT-REG)}$ threshold, the voltage regulation phase begins and the charging current begins to taper down.

If the battery is absent, the BAT pin cycles between charge done ($V_{O(REG)}$) and charging (battery recharge threshold, ~4.1 V).

As a safety backup, the VP8075 also monitors the charge time in the charge mode. If charge is not terminated within this time period, $t_{(CHG)}$, the VP8075 turns off the charger and enunciates FAULT on the $\overline{CHG}$ pin. See the DPPM operation under Case 1 for information on extending the safety timer during DPPM operation.

Temperature Regulation and Thermal Protection

In order to maximize charge rate, the VP8075 features a junction temperature regulation loop. If the power dissipation of the IC results in a junction temperature greater than the $T_{J(REG)}$ threshold, the VP8075 throttles back on the charge current in order to maintain a junction temperature around the $T_{J(REG)}$ threshold. To avoid false termination, the termination detect function is disabled while in this mode.

The VP8075 also monitors th e junction temperature, T_J, of the die and disconnects the OUT pin from the IN input if T_J exceeds $T_{(SHTDWN)}$. This operation continues until T_J falls below $T_{(SHTDWN)}$ by the hysteresis level specified in the specification table.

The battery supplement mode has no thermal protection. The Q2 FET continues to connect the battery to the output (system), if input power is not sufficient; however, a short-circuit protection circuit limits the battery discharge current such that the maximum power dissipation of the part is not exceeded under typical design conditions.

Charge Timer Operation

As a safety backup, the VP8075 monitors the charge time in the charge mode. If the termination threshold is not detected within the time period, $t_{(CHG)}$, the VP8075 turns off the charger and enunciates FAULT on the $\overline{CHG}$ pin. The resistor connected between the TMR and VSS, R_{TMR}, determines the timer period. The $K_{(TMR)}$ parameter is specified in the specifications table. In order to disable the charge timer, eliminate R_{TMR}, connect the TMR pin directly to the a VSS pin. Note that this action eliminates all safety timers, and also clears any timer fault.

$$t_{(CHG)} = K_{(TMR)} \times R_{(TMR)} \qquad (4)$$

While in the thermal regulation mode or DPPM mode, the VP8075 dynamically adjusts the timer period in order to provide the additional time needed to fully charge the battery. This proprietary feature is designed to prevent against early or false termination. The maximum charge time in this mode, $t_{(CHG-TREG)}$, is calculated by Equation 5.

$$t_{(CHG-TREG)} = \frac{t_{(CHG)} \times V_{(SET)}}{V_{(SET-REG)}} \qquad (5)$$

Note that because this adjustment is dynamic and changes as the ambient temperature changes and the charge level changes, the timer clock is adjusted. It is difficult to estimate a total safety time without integrating the above equation over the charge cycle. Therefore, understanding the theory that the safety time is adjusted inversely proportionately with the charge current and the battery is a current-hour rating, the safety time dynamically adjusts appropriately.

$K_{(SET-TREG)}$ is current factor during the thermal regulation or DPPM mode and is a function of charge current. (Note that charge current is dynamically adjusted during the thermal regulation or DPPM mode.)

$$I_{O(BAT)} = \frac{K_{(SET-TREG)}}{R_{SET}} \qquad (6)$$

All de-glitch times also adjusted proportionally to $t_{(CHG-TREG)}$.

Dynamic Charge Timers (TMR Input)

The VP8075 devices contain internal safety timers for the pre-charge and fast-charge phases to prevent potential damage to the battery and the system. The timers begin at the start of the respective charge cycles. The timer values are programmed by connecting a resistor from TMR to VSS. The resistor value is calculated using the following equation:

$$t_{PRECHG} = K_{TMR} \times R_{TMR}$$
$$t_{MAXCHG} = 10 \times K_{TMR} \times R_{TMR} \qquad (7)$$

Leave TMR unconnected to select the internal default timers. Disable the timers by connecting TMR to VSS. Note that timers are suspended when the device is in thermal shutdown, and the timers are slowed proportionally to the charge current when the device enters thermal regulation.

If the pre charge timer expires before the battery voltage reaches V_{LOWV}, the VP8075 indicates a fault condition. Additionally, if the battery current does not fall to I_{TERM} before the fast charge timer expires, a fault is indicated. The $\overline{CHG}$ output flashes at approximately 2Hz to indicate a fault condition.

Charge Termination and Recharge

The VP8075 monitors the voltage on the ISET pin, during voltage regulation, to determine when termination should occur (80 – 250 mV). Once the termination threshold, $I_{(TERM)}$, is detected the VP8075 terminates charge. The resistor connected between the ISET and VSS, RSET, programs the fast charge current level, V_{ISET}=2.5V) and thus the C/10 and C/30 current termination threshold level.

After charge termination, the VP8075 re-starts the charge once the voltage on the BAT pin falls below the $V_{(RCH)}$ threshold. This feature keeps the battery at full capacity at all times.

Sleep and Standby Modes

The VP8075 charger circuitry enters the low-power sleep mode if the input is removed from the circuit. This feature prevents draining the battery into the VP8075 during the absence of input supply. Note that in sleep mode, Q2 remains on (i.e., battery connected to the OUT pin) in order for the battery to continue supplying power to the system.

The VP8075 enters the low-power standby mode if while input power is present, the EN1=EN2 input is high. In this suspend mode, internal power FET Q1 is turned off, the BAT input is used to power the system through the OUT pin. This feature is designed to limit the power drawn from the input supply (such as USB suspend mode).

Power Down

The VP8075 family remains in power down mode when the input voltage at the IN pin is below the undervoltage threshold (UVLO).

The Q1 FET connected between IN and OUT pins is off, and the status outputs $\overline{CHG}$ and $\overline{PG}$ are high impedance. The Q2 FET that connects BAT to OUT is ON. During power down mode, the short circuitry is active and monitors for overload conditions on OUT.

Power On

When V_{IN} exceeds the UVLO threshold, the VP8075 powers up. While V_{IN} is below V_{BAT} + $V_{(SLPENT)}$. The Q1 FET connected between IN and OUT pins is off, and the status outputs $\overline{CHG}$ and $\overline{PG}$ are high impedance. The Q2 FET that connects BAT to OUT is ON. During sleep mode, the short circuitry is active and monitors for overload conditions on OUT.

One V_{IN} rises above V_{BAT} + $V_{(SLPEXIT)}$, $\overline{PG}$ is driven low to indicate the valid power status. The device enters standby mode if (EN1 = EN2 = High). In standby mode, Q1 is OFF and Q2 is ON so OUT is connected to the battery input. During standby mode, the short circuitry is active and monitors for overload conditions on OUT.

When the input voltage at IN is within the valid range: V_{IN} > UVLO AND V_{IN} > V_{BAT} + $V_{(SLPEXIT)}$ AND V_{IN} < V_{OVP}, and the EN1 and EN2 pins indicate that the USB suspend mode is not enabled [(EN1, EN2) ≠ (High, High)] all internal timers and other circuit blocks are activated. The FET Q1 switches to the current limit threshold set by EN1, EN2 and R_{ILIM} and the device enters into the normal operation. During normal operation, the system is powered by the input source (Q1 is on), and the device continuously monitors the status of CE, EN1 and EN2 as well as the input voltage conditions. Q2 is turned on to charge the battery and whenever the input source cannot deliver the required load current (supplement mode).

Charge Status Outputs

The open-drain (OD) $\overline{CHG}$ outputs indicate various charger operations as shown in Table 2. These status pins can be used to drive LEDs or communicate to the host processor. Note that OFF indicates the open-drain transistor is turned off. Note that this assumes $\overline{CE}$ = Low.

Table 2. Status Pins Summary

CHARGE STATE	$\overline{CHG}$
Precharge in progress	ON
Fast charge in progress	ON
Charge done	OFF
Charge suspend(temperature), timer fault, and sleep mode	OFF

$\overline{PG}$, Outputs (Power Good)

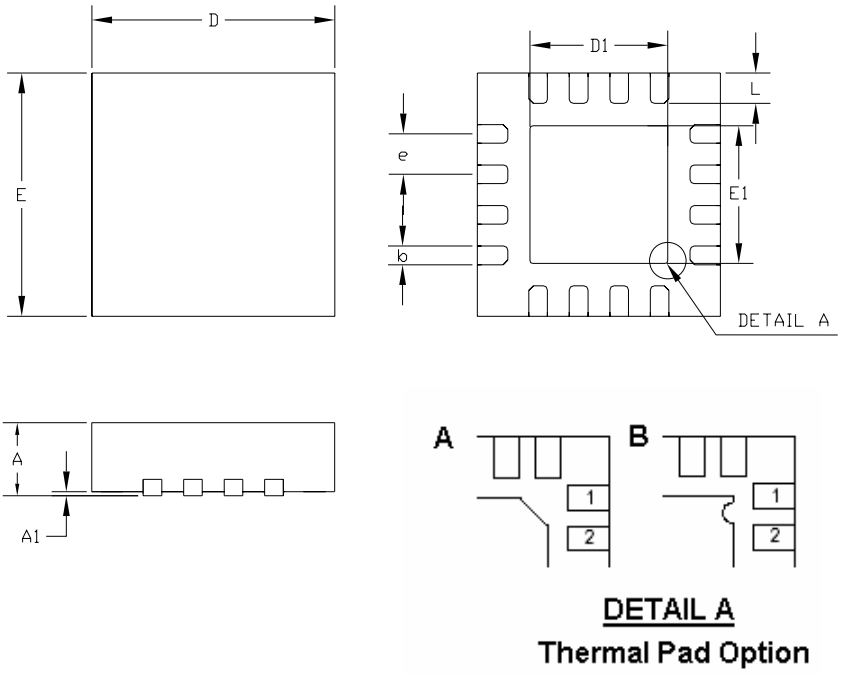
The open-drain pin, $\overline{PG}$, indicates when input power is present, and above the battery voltage. The corresponding output turns ON (low) when exiting sleep mode (input voltage above battery voltage). This output is turned off in the sleep mode (open drain). The $\overline{PG}$ pin can be used to drive an LED or communicate to the host processor. Note that OFF indicates the open-drain transistor is turned off.

SYSOFF

The VP8075 feature a SYSOFF input that allows the user to turn the FET Q2 off and disconnect the battery from the OUT pin. This is useful for disconnecting the system load from the battery. The $\overline{CHG}$ output remains low when SYSOFF is high. Connect SYSOFF to VSS, to turn Q2 on for normal operation. SYSOFF is internally pulled to VBAT.

Packaging Information

TQFN-16



SYMBOLS	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
b	0.18	0.30	0.007	0.012
E	2.90	3.10	0.114	0.122
D	2.90	3.10	0.114	0.122
D1	1.70		0.067	
E1	1.70		0.067	
e	0.50		0.020	
L	0.30	0.50	0.012	0.020